## CLAIMS

WHAT IS CLAIMED IS:

1. A 4-2 compressor for generating a sum bit and a carry bit as a result of four input data bits comprising:

a first logic circuit for performing a NAND operation and a NOR operation of a first and second input data, for generating an XOR/XNOR operation result of the first and second input data using the NAND and NOR operation results, and for generating a carry-out bit for a following stage by selecting either the NAND operation result or the NOR operation result;

a second logic circuit for generating a selection signal in response to a third input data, a fourth input data and the XOR/XNOR operation result from the first logic circuit;

a third logic circuit for generating the sum bit by selecting one of a carry-input bit and an inverted carry-input bit in response to the selection signal from the second logic circuit; and

a fourth logic circuit for generating the carry bit by selecting one of the inverted carry-input bit and an inverted fourth input data in response to the selection signal from the second logic circuit.

2. The 4-2 compressor according to claim 1, wherein the first logic circuit comprises:

a first XOR/XNOR logic circuit for performing the NAND operation and the NOR operation, respectively, and for generating the XOR/XNOR operation result by using the NAND and NOR operation results; and

a first multiplexer for generating the carry-out bit for the following stage by selecting either the NAND operation result or the NOR operation result in response to an inverted third data, wherein the first multiplexer is a single railed multiplexer.

3. The 4-2 compressor according to claim 1, wherein the second logic circuit comprises:

a second XOR/XNOR logic circuit for performing a NAND operation and a NOR operation of the third input data and fourth input data, and for generating an XOR/XNOR operation result of the third and fourth input data by using the NAND and NOR operation results; and

a second multiplexer for generating the selection signal by selecting either the XOR operation result or the XNOR operation result from the first logic circuit, in response to the XOR/XNOR operation result from the second XOR/XNOR logic circuit, wherein the second multiplexer is a dual railed multiplexer.

4. The 4-2 compressor according to claim 1, wherein the third logic circuit comprises a third multiplexer for generating the sum bit, by selecting one of the carry-input bit and the inverted carry-input bit, in response to the selection signal from the second logic circuit, wherein the third multiplexer is a single railed multiplexer.

5. The 4-2 compressor according to claim 1, wherein the fourth logic circuit comprises a fourth multiplexer for generating the carry bit, by selecting one of the inverted fourth input data and the inverted carry-input bit, in response to the selection signal from the second logic circuit, wherein the fourth multiplexer is a single railed multiplexer.

6. The 4-2 compressor according to claim 2, wherein each XOR/XNOR logic circuit comprises:

a NAND gate for performing the NAND operation of a first data and a second data;

a NOR gate for performing the NOR operation of the first data and the second data;

an XNOR means for generating an XNOR result of the first and the second data in response to the outputs of the NOR gate and the NAND gate; and

an XOR means for generating an XOR result of the first and the second data in response to the outputs of the NOR gate and the NAND gate.

7. The 4-2 compressor according to claim 6, wherein the XNOR means comprises:

a first inverter for inverting the output from the NAND gate while the output of the NOR gate is a first logic state, and outputting the output from the NAND gate without inverting while the output of the NOR gate is a second logic state; and

a first full-swing means for making full-swing the output of the first inverter.

8. The 4-2 compressor according to claim 6, wherein the XOR means comprises:

a second inverter for inverting the output from the NOR gate while the output of the NAND gate is the second logic state, and outputting the output from the NAND gate without inverting while the output of the NOR gate is the second logic state; and

a second full-swing means for making full-swing the output of the second inverter.

9. The 4-2 compressor according to claim 7, wherein the first inverter comprises a P type transistor and a N type transistor having a current path between a power supply voltage source and an output port of the NOR gate in series, and a control electrode controlled by the output of the NAND gate.

10. The 4-2 compressor according to claim 7, wherein the first full-swing means comprises a P type transistor having a current path between an output port of the first inverter and the output port of the NOR gate, and control electrode controlled by the first data.

11. The 4-2 compressor according to claim 10, wherein the first full-swing means is turned on when the output signal of the NOR gate is the second logic level, and increases the voltage level of the output signal of the first inverter as high as the power supply voltage level.

12. The 4-2 compressor according to claim 8, wherein the second inverter comprises a P type transistor and a N type transistor having a current path between a ground voltage source and an output port of the NAND gate in series, and a control electrode controlled by the output of the NOR gate.

13. The 4-2 compressor according to claim 8, wherein the second full-swing means comprises a N type transistor having a current path between an output port of the second inverter and the output port of the NAND gate, and control electrode controlled by the first data.

14. A 4-2 compressor according to claim 13, wherein the second full-swing means is turned on when the output signal of the NAND gate is the first logic level, and decreases the voltage level of the output signal of the second inverter as low as the ground voltage level.

15. The 4-2 compressor according to claim 3, wherein each XOR/XNOR logic circuit comprises:

a NAND gate for performing the NAND operation of a first data and a second data;

a NOR gate for performing the NOR operation of the first data and the second data;

an XNOR means for generating an XNOR result of the first and the second data in response to the outputs of the NOR gate and the NAND gate; and

an XOR means for generating an XOR result of the first and the second data in response to the outputs of the NOR gate and the NAND gate.

16. A 4-2 compressor for generating a sum bit and a carry bit as a result of four input data bits comprising:

a first XOR/XNOR logic circuit for performing a NAND operation and a NOR operation of a first and second input data, for generating an XOR/XNOR operation result of the first and second input data by using the NAND and NOR operation results;

a first multiplexer for generating the carry-out bit for following stage by selecting either the NAND operation result of the NOR operation result in response to an inverted third input data, wherein the first multiplexer is a single railed multiplexer;

a second XOR/XNOR logic circuit for performing a NAND operation and a NOR operation of a third input data and fourth input data, and for generating an XOR/XNOR operation result or the third and fourth input data by using the NAND and NOR operation results;

a second multiplexer for generating the selection signal by selecting either the XOR operation result or the XNOR operation result from the first XOR/XNOR logic circuit, in response to the XOR/XNOR operation result from the second XOR/XNOR logic circuit, wherein the second multiplexer is a dual railed multiplexer;

a third multiplexer for generating the sum bit, by selecting one of a carry-input bit and inverted carry-input bit, in response to the selection signal from the second multiplexer, wherein the third multiplexer is a single railed multiplexer; and

a fourth multiplexer for generating the carry bit, by selecting one of an inverted fourth input data and the inverted carry-input bit, in response to the selection signal from the second multiplexer, wherein the fourth multiplexer is a single railed multiplexer.